The Effect of Reduced Oxidation Process Using Ammonia Annealing and Deposited Oxides on 4H-SiC Metal-Oxide-Semiconductor Structure

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Nitric oxide (NO) post-oxidation annealing (POA) is an effective method for lowering the carbon component at an oxide/4H-SiC interface. However, this method has a drawback of additional oxidation by oxygen source from the NO gas. Atomic-layer-deposited (ALD) oxides subjected to ammonia (NH₃) annealing were employed to realize nitridation without oxidation process. Because NH₃-annealed oxides have a drawback of high leakage current, deposition of dielectrics on ALD SiO₂ with subsequent NH₃ annealing were performed to reduce leakage current and to prevent oxidation, respectively. The employments of this process reduced interface trap density and surface roughness effectively while maintaining low leakage current.

4H-SiC is a promising wide-band-gap material with superior electrical, chemical, and thermal properties. Because of these characteristics, it attracts great interest for use in high-power, high-frequency, and high-temperature applications. However, the 4H-SiC metal-oxide-semiconductor MOS structure has some drawbacks such as high interface trap density which result from residual carbon, carbon clusters, and dangling bonds at the SiO₂/4H-SiC interface. These traps are generated during thermal oxidation and reduce the channel mobility of 4H-SiC MOS field-effect transistors (FETs). Nitridation using nitric oxide (NO) or nitrous oxide (N₂O) gas is an effective method for mitigating these problems at oxide/silicon interfaces; however, this method is not sufficient to reduce carbon-related defects.

In this study, we adopted ALD SiO₂ with NH₃ PDA to obtain a nitrided SiO₂/4H-SiC interface without oxidation. NH₃ annealing is considered an effective method for reducing Dₙ and effective oxide charge (Qₑ) by an order of magnitude. However, it induces a large amount of nitrogen throughout the oxide; therefore, it significantly changes the oxide stoichiometry and decreases the breakdown field (Eₑ). This low breakdown field is the main drawback of NH₃ annealing and is the reason why it has not been studied as much as NO-based post-oxidation annealing (POA). Therefore, in the current study, the deposited dielectrics, high-density plasma chemical vapor deposition (HDPCVD) SiO₂ and ALD Al₂O₃, on ALD SiO₂ with NH₃ annealing were attempted to reduce leakage current while maintaining oxidation-free SiO₂/4H-SiC interface.

MOS capacitors were fabricated with a 12-μm-epitaxial layer, doped with 5 × 10¹⁵ cm⁻³ of nitrogen, on Si-face n-type 4H-SiC wafers. A standard wafer cleaning process (RCA) was carried out prior to oxide growth for improving the interface quality. Thereafter, a wet oxidation process at 1100 °C was performed for 2 h for obtaining a thermally grown oxide (denoted as “T” hereafter). For obtaining ALD oxides, SiO₂ films were deposited by ALD using SiH₄[N(C₂H₅)₂]₂ [bis(diethylamino)silane] and O₂ plasma as a precursor and reactant, respectively (denoted as “A” hereafter). Before the ALD growth, the same cleaning process was used. The ALD chamber pressure and substrate temperature were kept at 3 Torr and 280 °C, respectively. NO and NH₃ gas annealing were performed for 2 h at 1175 °C and 1100 °C, respectively (denoted respectively as “NO” and “NH₃”, hereafter). During the cooling to 800 °C for about 2.5 h, Ar gas flow was maintained. The thickness of all oxide layers was evaluated by spectroscopic ellipsometer. The thickness of both thermally grown and ALD SiO₂ after being subjected to NO PDA was 28 nm. The thickness of ALD SiO₂ subjected to NH₃ gas annealing was 15 nm. HDPCVD SiO₂ with a thickness of 25 nm (denoted as “H” hereafter) was deposited on NH₃-annealed SiO₂. The HDPCVD was performed using SiH₄, O₂, and Ar gases at the substrate temperature of 250 °C. The process pressure was 3 mTorr and the deposition rate was 10 Å/s. ALD Al₂O₃ was also deposited on NH₃-annealed ALD SiO₂ by using trimethylaluminum (TMA) as a precursor and H₂O as a reactant at 310 °C. 100 nm-thick Ni gate electrode was formed by sputtering and the area was defined to be 1.3 × 10⁻⁴ cm² by photolithography. Backside Ohmic contact was prepared by thermal evaporation of 100 nm-thick Al. All the metal depositions were carried out without additional substrate heating. The capacitance–voltage (C–V) characteristics were measured using an HP4140 and Dₓ was measured via the conductance method by using an HP4124. Conductance method provided the Dₓ which is linearly proportional to the peak value of a conductance as a function of measured frequency at room temperature. The current density–electric field (J–E) characteristics were measured by the time-zero dielectric breakdown (TZDB) test carried out using an HP4155A analyzer. J–E characteristics were analyzed from eight MOS structures and the electric field was calculated by dividing applied voltage with total oxide thickness. Chemical profiles of the oxides were obtained by time-of-flight secondary ion mass spectroscopy (ToF-SIMS). The ToF-SIMS data were acquired using 8 keV Cs⁺ ion bombardment while monitoring clustered secondary species of the M⁺ Cs⁻ form.

Figures 1a and 1b show the temperature dependence of the J–E characteristics of ALD SiO₂ before and after NO PDA. The current of as-deposited ALD SiO₂ did not vary much with temperature changes. After NO PDA, in contrast, the current in a medium electric field (2–6 MV/cm) showed a gradual increase as the temperature increased from 300 K to 390 K. Such temperature dependence of the current was attributed to the Pool-Frenkel conduction mechanism in addition to the Fowler-Nordheim tunneling in this region (data not shown). Similar mixed conduction behavior was also recently reported by Sometani et al. This phenomenon indicates additional oxidation of a newly grown oxide during NO PDA induces trap sites. Moreover,
the increased oxide thickness (from 22 nm to 28 nm) supports that NO PDA introduces oxygen at the SiO2/4H-SiC interface. This oxygen leads to additional oxidation of SiC, which is the major drawback of NO PDA.10

To avoid this oxidation problem, NH3 PDA was investigated as an alternative gas ambient to NO. First, an ALD SiO2 layer with a thickness of 15 nm was deposited; this was followed by NH3 PDA to form a nitried dielectric layer without oxidation process. J–E measurements revealed that such an oxide obtained after NH3 PDA shows much larger leakage current than that obtained after NO POA (data not shown). To block the leakage current originated from NH3 annealing, an additional 13-nm-thick ALD SiO2 layer was deposited. Inert gas annealing (IGA) using Ar gas (denoted as “I” hereafter), generally used to reduce the number of defect states in as-deposited oxides, was conducted for 1 h at 1175 °C for curing the upper ALD SiO2 layer. From J–E characteristics, we already confirmed that ALD SiO2 layer with IGA (A+I) exhibits a good insulator (data not shown). However, the A+NH3+A+I stack showed very high leakage current at 300 K, contrary to our expectation (Fig. 2a). The data acquired for constructing C–V curves was not reliable owing to such high leakage current. For comparison, the same process (NH3+A+I) was repeated using the thermal oxide as the starting material instead of ALD SiO2 (T+NH3+A+I), and it showed slightly better leakage properties. However, all these oxides were still very inferior to thermal and ALD oxides obtained after NO POA (T+NO and A+NO, respectively, in Fig. 2a). Such high leakage current of the A+NH3+A+I stack may have originated from nitrogen incorporation into the defective lower and/or upper ALD SiO2 layer. This is clearly shown in the ToF–SIMS depth profile in Fig. 2b. The stacked structure obtained by subjecting ALD SiO2 to NH3 PDA (A+NH3+A+I) showed much larger nitrogen amount than ALD SiO2 subjected to NO PDA only (A+NO) as well as the thermal-oxide–based stack (T+NH3+A+I). It appears that NO PDA induced only a small amount of nitrogen, and this nitrogen passivated defects only at the oxide/4H-SiC interface. However, nitrogen originating from NH3 annealing appeared to spread throughout the entire ALD SiO2 layer; moreover, its amount was higher than that in the case of thermally grown SiO2. This large nitrogen amount was not only incorporated into the lower ALD SiO2 layer but also diffused to the upper additional ALD SiO2 layer after high-temperature IGA. Therefore, it can be concluded that an additional ALD SiO2 layer with Ar IGA (A+I) is not effective for reducing leakage current. Mobile hydrogen ion (H+) incorporated during NH3 annealing could also be the cause of high leakage current. However, it was confirmed using double sweep C–V that little amount of mobile ions including H+ is left inside the oxide after NH3 annealing. It is believed that Ar flow during 2.5 h cooling effectively removed mobile ions, as reported by Chanthaphan et al.21 and Jung et al.22 Therefore, nitrogen incorporation into the defective ALD SiO2 is the main cause of the inferior leakage behavior.

Another structure of bilayer SiO2, HDPCVD SiO2 on ALD SiO2, was also employed to reduce leakage current (A+NH3+H). HDPCVD SiO2 is more stable than ALD SiO2; even though the former is obtained without high-temperature annealing.23,24 In addition, an ALD Al2O3 layer was tested as an upper dielectric layer to reduce leakage current by restricting the nitrogen accumulation region (A+NH3+Al2O3). Al2O3 is deposited ideally by ALD, and it has good thermal stability with low leakage current.21 Forming gas (5%-H2/95%-N2) annealing (FGA, denoted as “F” hereafter) was carried out after Al2O3 deposition for 1 h at 800 °C; this process is known to eliminate dangling bonds and fixed charges in the Al2O3 layer (finally, A+NH3+Al2O3+F).26,27 An annealing temperature of 800 °C was selected to minimize nitrogen diffusion to the upper ALD oxide layer. The J–E characteristics in Fig. 3a show that the upper HDPCVD SiO2 or ALD Al2O3 layer considerably decreased the leakage current level compared to the stack with an upper ALD SiO2 layer, especially in the soft breakdown region. Therefore, this stacked structure containing an HDPCVD SiO2 or ALD Al2O3 upper layer showed better dielectric characteristics than that containing ALD SiO2 with

Figure 1. J–E characteristics of ALD SiO2 obtained (a) before and (b) after NO PDA.

Figure 2. (a) J–E characteristics and (b) ToF–SIMS profile of stacked oxide structures containing ALD SiO2 subjected to IGA. The characteristics of thermally grown SiO2 and ALD SiO2 subjected to NO PDA are given for reference.
IGA (A+I). The reduced leakage current level enabled us to evaluate the interface characteristics of NH3-annealed SiO2/4H-SiC, which did not undergo the detrimental additional oxidation process. The $D_i$ distribution for the stacked structure containing HDPCVD SiO2 or ALD Al2O3 on NH3-annealed ALD SiO2 extracted by the conductance method is shown in Fig. 3b. It can be seen that stacks containing HDPCVD SiO2 or ALD Al2O3 subjected to FGA exhibited lower $D_i$ than that containing ALD SiO2 with NO annealing (A+NO). We believe that NH3 annealing, which formed a nitrided SiO2 layer without oxidation process, lowered $D_i$ (Fig. 3b), and the upper additional dielectric layer with superior properties (HDPCVD SiO2 or ALD Al2O3) maintained good leakage characteristics (Fig. 3a).

The surface roughness of 4H-SiC induces mobility degradation. Some studies have reported an increase in the surface roughness of 4H-SiC after oxidation, and attributed this increase to the formation of carbon clusters and/or silicon oxy carbides during oxidation. Low-temperature and suppressed oxidation of a stacked structure with an upper HDPCVD SiO2 or ALD Al2O3 layer results in low $D_i$ as well as a smoother 4H-SiC surface.9,31–33 Figure 4 shows the atomic force microscopy (AFM) images of 4H-SiC, after the removal of all oxide layers by using HF.

**Figure 3.** (a) $J$–$E$ characteristics and (b) $D_i$ distribution of stacked oxide structures containing HDPCVD SiO2 or Al2O3 subjected to FGA. The characteristics of ALD SiO2 subjected to NO PDA and thermally grown SiO2 are given for reference.

**Figure 4.** AFM images of 4H-SiC after the removal of all oxide layers by using HF.

In summary, a facile method to avoid the generation of carbon-related defects and a rough interface at an oxide/4H-SiC interface was established. NH3 annealing was investigated to replace the conventional NO annealing process, which has a detrimental oxidation problem. A thin ALD SiO2 layer subjected to NH3 PDA was used to maintain low $D_i$ without oxidation. However, NH3 annealing led to the increased leakage current. An additional HDPCVD SiO2 or ALD Al2O3 layer subjected to FGA provided good leakage properties to the whole oxide stack. The NH3 nitridation method proposed herein can avoid detrimental oxidation and it preserves a smooth 4H-SiC surface, suggesting that it could be a viable alternative to NO PDA.

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**References**